REMARKS

Examiner's Note

Claims 4, 7, 11, 12, 16, 18, 25, 28, 32, 33 and 35 were objected to as based on the "and" term included in the claim. The "and" is herein replaced by the term "or". The prior amendment was merely a typographical error, and the Applicant thanks the Examiner for pointing out this typographical error.

35 USC § 112

Claims 2, 7 (now cancelled), 12, 15, 16, 23 28 (now cancelled) and 33 were rejected under 35 USC §112 as containing subject matter that was not described in the specification. The Applicant disagrees, especially in view of the amendments made herein.

Claims 2, 12, 15, 16, 23 and 33 are herein amended to replace the term "and" with the term "or". Based on this reason, among others, claims 2, 12, 15, 16, 23 and 33 should be deemed allowable.

35 USC § 103

Claims 1-6, 8-11, 13-15 and 17-27, 29-32 and 34-38 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and Pellerin et al. The Applicant disagrees, especially in view of the amendments presented herein.

Claim 1 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, **wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide**; b) forming a via opening in said stack; c) depositing a sacrificial inorganic dielectric in the via

opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a line opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, **wherein the hardmask layer comprises a material comprising silicon oxynitride *or* silicon oxide**; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and substantially covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material.

The methods taught in the admitted prior art, Avanzino or Pellerin do not teach or suggest that the hardmask layer comprises silicon oxinitride or silicon oxide. There is also nothing in the description of the admitted prior art, Avanzino or Pellerin that would teach or suggest that the hardmask layer comprises silicon oxinitride or silicon oxide. The methods taught in the admitted prior art, Avanzino or Pellerin would also not motivate one ordinarily skilled in the art of interconnect assembly to apply a hardmask layer that comprises silicon oxinitride or silicon oxide.

Based on these arguments, among others, claims 1 and 22 are allowable as being patentable over the admitted prior art and Avanzino in view of Pellerin. Further, claims 2-6, 8-11, 13-15, 17-21, 23-27, 29-32 and 34-38 are also allowable as being dependent on independent claims 1 and 22.

CHANGE OF FIRM NAME

For your immediate reference, the firm of Fish & Associates, LLP – which may have been recently listed on the correspondence for the Applicant – has merged with the law firm of Rutan & Tucker, LLP to collectively become the law firm of Rutan & Tucker, LLP as of January 1, 2002. Completed Change of Correspondence Address forms for this matter, showing the new address listed below, will be submitted this month to the USPTO. New Power of Attorney forms will not need to be filed, however, since the Attorneys of Record have not changed through this merger.

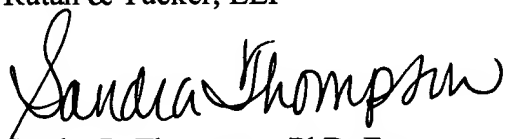
REQUEST FOR ALLOWANCE

Claims 1-6, 8-27 and 29-38 are pending in this application. The applicant requests allowance of all pending claims.

Respectfully submitted,

Rutan & Tucker, LLP

Dated: December 23, 2002

By: 

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MARKED UP COPY OF PENDING CLAIMS

1. (Twice Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide;

forming a via opening in said stack;

depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially filling the via opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a line opening in the stack and the sacrificial inorganic dielectric, said line opening substantially aligned with said via opening;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

2. (Twice Amended) The method of Claim 1 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, [and] or mixtures thereof.

3. The method of Claim 1 wherein said sacrificial inorganic dielectric is a methylsiloxane.

4. (Twice Amended) The method of Claim 1, wherein the organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, [and] or mixtures thereof.

5. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

6. The method of Claim 5 wherein said diffusion barrier layer comprises silicon nitride.

7. Cancelled.

8. The method of Claim 1 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

9. The method of Claim 8 wherein said diffusion barrier layer comprises silicon nitride.

10. The method of claim 8, wherein the etchstop layer comprises a material comprising silicon oxide.

11. (Twice Amended) The method of Claim 8, wherein the second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, [and] or mixtures thereof.

12. (Twice Amended) The method of claim 8, wherein the hardmask layer on said second intermetal dielectric layer comprises a material comprising silicon oxynitride [and] or silicon oxide.

13. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer on said substrate, and inorganic intermetal dielectric layer between said diffusion barrier and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

14. The method of Claim 13 wherein said diffusion barrier layer comprises silicon nitride.

15. (Twice Amended) The method of clam 13 wherein said inorganic intermetal dielectric layer comprises a material that comprises silicon oxide, fluorinated silicate glass, or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, [and] or mixtures thereof.

16. (Twice Amended) The method of claim 13, wherein the hardmask layer comprises a material comprising silicon oxynitride [and] or silicon oxide.

17. The method of Claim 1 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

18. (Twice Amended) The method of Claim 1 wherein said conducting material comprises aluminum, copper, tungsten, [and] or mixtures thereof.

19. The method of Claim 18 wherein said conducting material further comprises a conducting diffusion barrier material.

20. The method of Claim 1 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

21. The method of Claim 1 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.

22. (Twice Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride *or* silicon oxide;

forming a line opening in said stack;

depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a via opening in the stack and the sacrificial inorganic dielectric;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

23. (Twice Amended) The method of Claim 22 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, [and] or mixtures thereof.

24. The method of Claim 22 wherein said sacrificial inorganic dielectric is a methylsiloxane.

25. (Twice Amended) The method of Claim 22, wherein the organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material

obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, [and] or mixtures thereof.

26. The method of Claim 22 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

27. The method of Claim 26 wherein said diffusion barrier layer comprises silicon nitride.

28. Cancelled.

29. The method of Claim 22 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

30. The method of Claim 29 wherein said diffusion barrier layer comprises silicon nitride.

31. The method of claim 29, wherein the etchstop layer comprises a material comprising silicon oxide.

32. (Twice Amended) The method of Claim 29, wherein the second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, [and] or mixtures thereof.

33. (Twice Amended) The method of Claim 29, wherein the hardmask layer comprises a material comprising silicon oxynitride [and] or silicon oxide.

34. The method of Claim 22 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

35. (Amended) The method of Claim 22 wherein said conducting material comprises aluminum, copper, tungsten, [and] or mixtures thereof.

36. The method of Claim 35 wherein said conducting material further comprises a conducting diffusion barrier material.

37. The method of Claim 22 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

38. The method of Claim 22 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.

CLEAN COPY OF PENDING CLAIMS

1. (Twice Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide;

forming a via opening in said stack;

depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially filling the via opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a line opening in the stack and the sacrificial inorganic dielectric, said line opening substantially aligned with said via opening;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

2. (Twice Amended) The method of Claim 1 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

3. The method of Claim 1 wherein said sacrificial inorganic dielectric is a methylsiloxane.

4. (Twice Amended) The method of Claim 1, wherein the organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

5. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

6. The method of Claim 5 wherein said diffusion barrier layer comprises silicon nitride.

7. Cancelled.

8. The method of Claim 1 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

9. The method of Claim 8 wherein said diffusion barrier layer comprises silicon nitride.

10. The method of claim 8, wherein the etchstop layer comprises a material comprising silicon oxide.

11. (Twice Amended) The method of Claim 8, wherein the second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

12. (Twice Amended) The method of claim 8, wherein the hardmask layer on said second intermetal dielectric layer comprises a material comprising silicon oxynitride or silicon oxide.

13. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer on said substrate, and inorganic intermetal dielectric layer between said diffusion barrier and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

14. The method of Claim 13 wherein said diffusion barrier layer comprises silicon nitride.

15. (Twice Amended) The method of clam 13 wherein said inorganic intermetal dielectric layer comprises a material that comprises silicon oxide, fluorinated silicate glass, or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

16. (Twice Amended) The method of claim 13, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide.

17. The method of Claim 1 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

18. (Twice Amended) The method of Claim 1 wherein said conducting material comprises aluminum, copper, tungsten, or mixtures thereof.

19. The method of Claim 18 wherein said conducting material further comprises a conducting diffusion barrier material.

20. The method of Claim 1 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

21. The method of Claim 1 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.

22. (Twice Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride *or* silicon oxide;

forming a line opening in said stack;

depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a via opening in the stack and the sacrificial inorganic dielectric;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

23. (Twice Amended) The method of Claim 22 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

24. The method of Claim 22 wherein said sacrificial inorganic dielectric is a methylsiloxane.

25. (Twice Amended) The method of Claim 22, wherein the organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material

obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

26. The method of Claim 22 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

27. The method of Claim 26 wherein said diffusion barrier layer comprises silicon nitride.

28. Cancelled.

29. The method of Claim 22 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

30. The method of Claim 29 wherein said diffusion barrier layer comprises silicon nitride.

31. The method of claim 29, wherein the etchstop layer comprises a material comprising silicon oxide.

32. (Twice Amended) The method of Claim 29, wherein the second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

33. (Twice Amended) The method of Claim 29, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide.

34. The method of Claim 22 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

35. (Amended) The method of Claim 22 wherein said conducting material comprises aluminum, copper, tungsten, or mixtures thereof.

36. The method of Claim 35 wherein said conducting material further comprises a conducting diffusion barrier material.

37. The method of Claim 22 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

38. The method of Claim 22 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.